AND8323

Compact, Dual 2 A Reference Design with the NCP3120

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Evaluation Board Specification:

Characteristic		Min	Typ	Max	Unit	Comments
Input Voltage		7		15	V	(Note 1)
Output Voltage	V_{out1}		3.3		V	
	V_{out2}		5		V	
Output Current	V_{out1}	0		2	A	
	V_{out2}	0		2	A	
Oscillator Frequency			300		kHz	
Enable Threshold High	EN Tied to SEQ	2.0			V	EN Tied to SEQ
Sequence Threshold Low	EN Tied to SEQ			0.8	V	EN Tied to SEQ
Voltage Ripple	V_{out1}		40		mV_{pk-pk}	
	V_{out2}		40		mV_{pk-pk}	
Load Regulation	V_{out1}		0.61		mV/A	
(V_{in} = 12 V, I_{out} = 0.5 – 2 A)	V_{out2}		0.21		mV/A	
Line Regulation	V_{out1}		1.85		mV/V	
(V_{in} = 10.8 – 13.2 V, I_{out} = 2 A)	V_{out2}		3.53		mV/V	
Thermal Shutdown			160		°C	
Dual 2 A DC–DC Converter Dimensions		1″ X 2″				Outlined Area

1. Operation down to 4.5 V requires selecting a lower voltage for V_{out2}.

Circuit Description

The NCP3120 operates as a voltage–mode, pulse–width–modulated, (PWM) asynchronous buck converter. Its operating frequency is adjustable with an external resistor to ground from 220 kHz to 750 kHz. minimum switching frequency of 220 kHz and a maximum 750 kHz. Also, an onboard operational transconductance amplifier (OTA) integrates the error signal to provide high DC accuracy. The NCP3120 also includes an enable and disable function with externally controlled soft start and stop.

Board Details

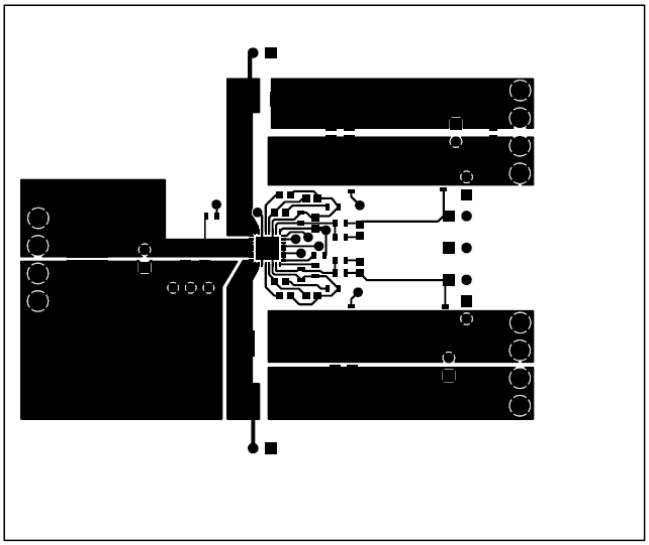

Figure 1. Top Layer

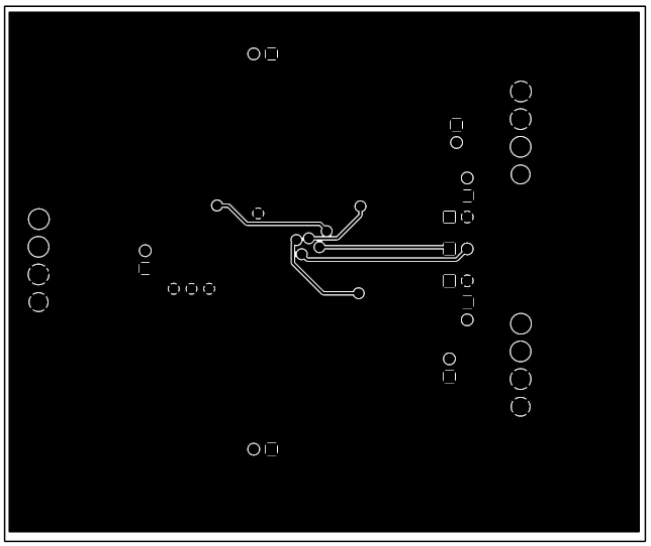

Figure 2. Bottom Layer

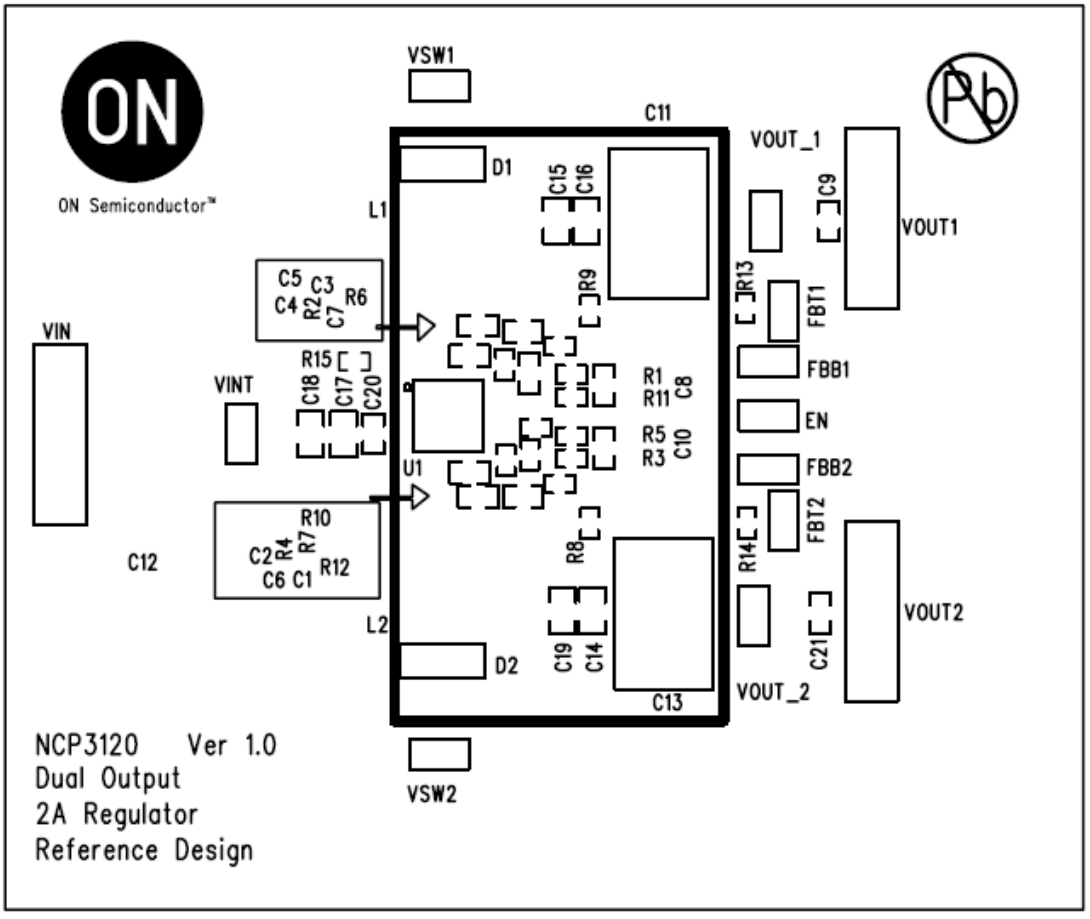

Figure 3. Silkscreen Layer

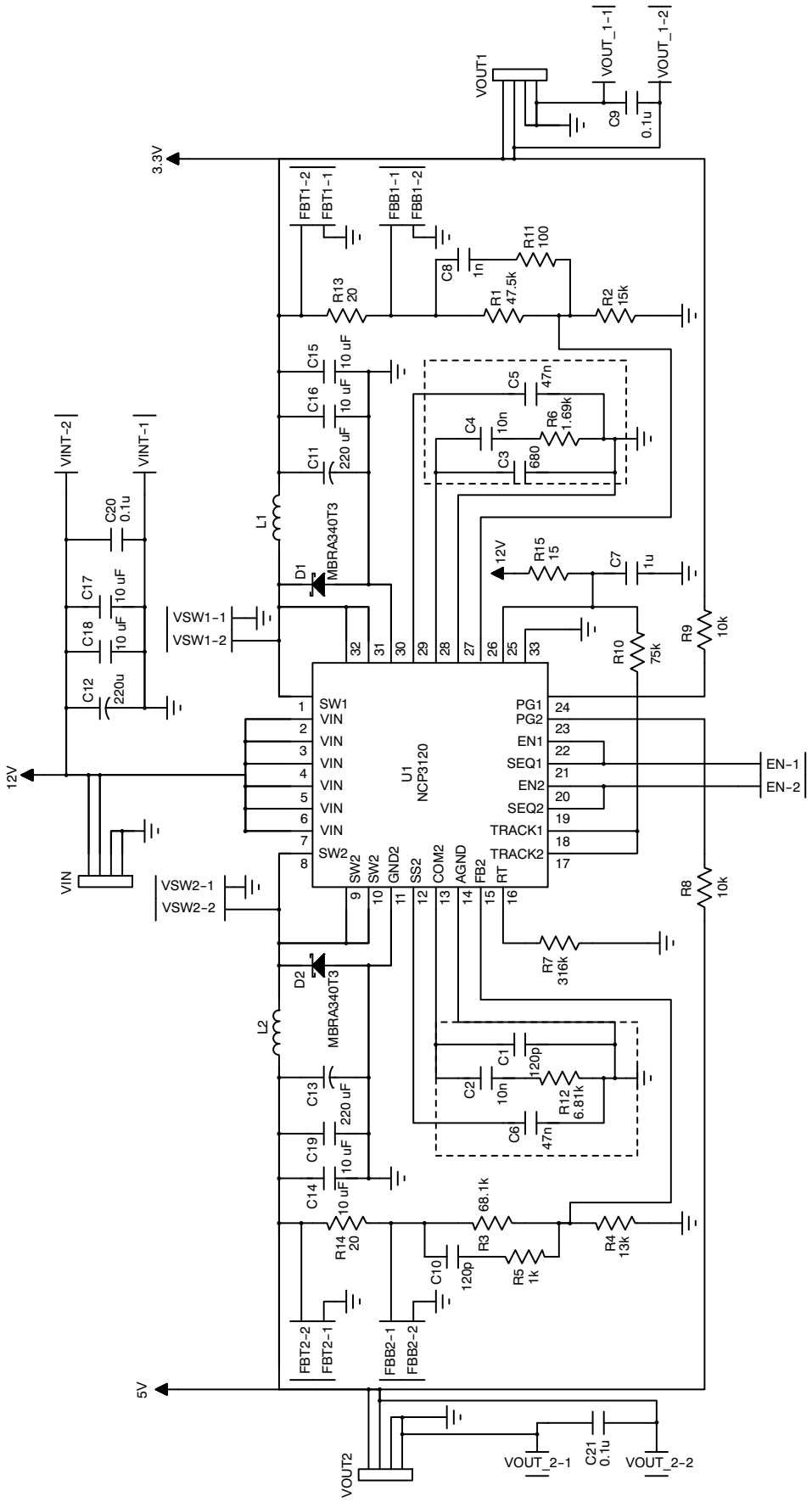

Figure 4. Evaluation Board − Schematic

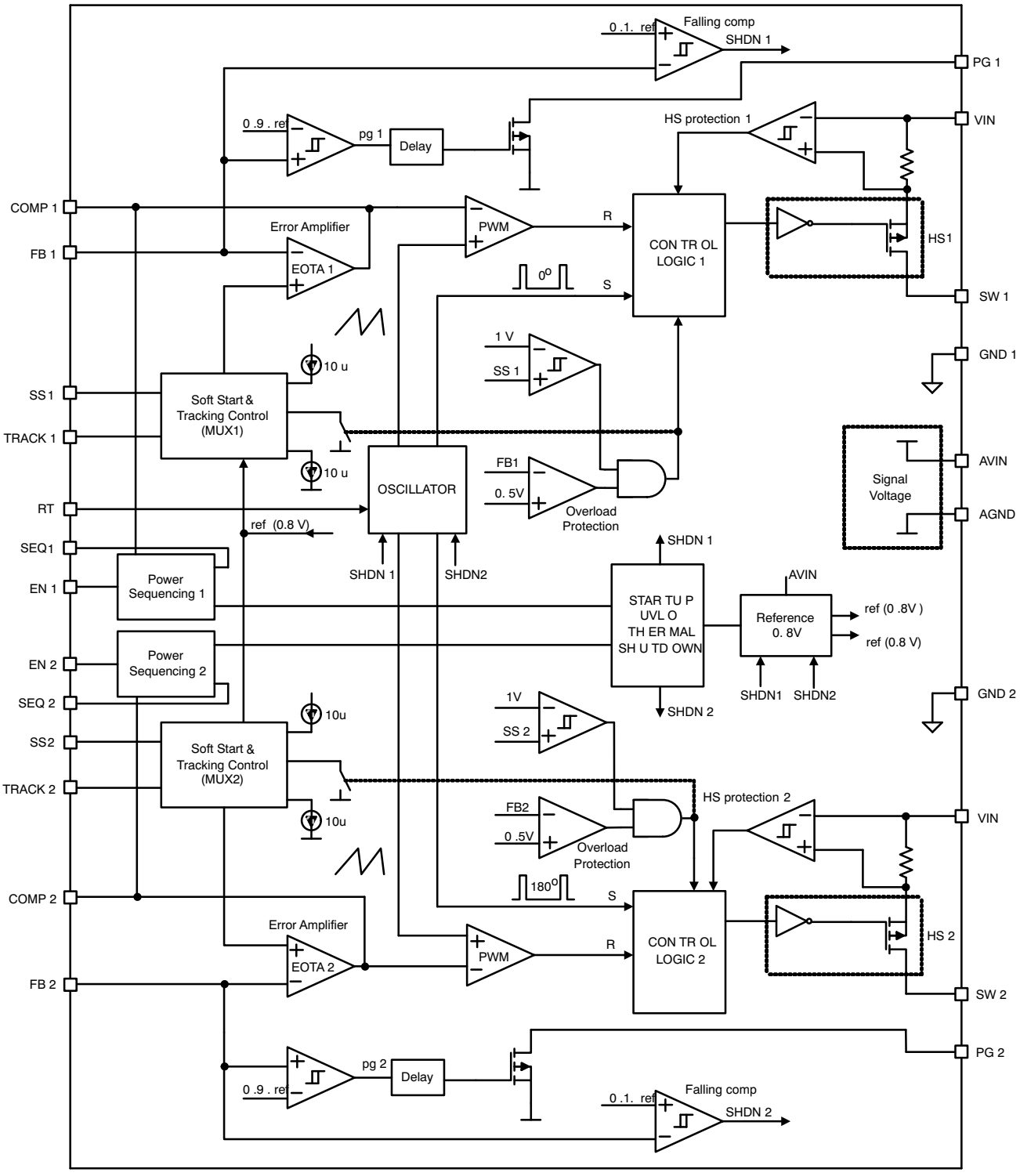

Figure 5. Block Diagram – NCP3120

PIN DESCRIPTION

Pin	Symbol	Description
1, 31, 32	SW1	Switch node of Channel 1. Connect an inductor between SW1 and the regulator output.
2 – 7	V_{IN}	Input power supply voltage pins. These pins should be connected together to the input signal supply voltage pin.
8 – 10	SW2	Switch node of Channel 2. Connect an inductor between SW2 and the regulator output.
11	GND2	Power ground for Channel 2
12	SS2	Soft−start control input for Channel 2. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
13	COMP2	Compensation pin of Channel 2. This is the output of the error amplifier and inverting input of the PWM comparator.
14	AGND	Analog ground; connect to GND1 and GND2.
15	FB2	Feedback Pin. Used to set the output voltage of Channel 2 with a resistive divider from the output.
16	RT	Resistor select for the oscillator frequency. Connect a resistor from the RT pin to AGND to set the frequency of the master oscillator.
17	TRACK 2	Tracking input for Channel 2. This pin allows the user to control the rise time of the second output. This pin must be tied high in the normal operation (except in the tracking mode).
18	TRACK 1	Tracking input for Channel 1. This pin allows the user to control the rise time of the first output. This pin must be tied high in the normal operation (except in the tracking mode).
19	SEQ2	Sequence pin for Channel 2. I/O used in power sequencing. Connect SEQ to EN for normal operation of a standalone device.
20	EN2	Enable input for Channel 2.
21	SEQ1	Sequence pin for Channel 1. I/O used in power sequencing. Connect SEQ to EN for normal operation of a standalone device.
22	EN1	Enable input for Channel 1.
23	PG2	Power good, open−drain output of Channel 2. Output logic is pulled to ground when the output is less than 90% of the desired output voltage. Tied to an external pull−up resistor.
24	PG1	Power good, open−drain output of Channel 1. Output logic is pulled to ground when the output is less than 90% of the desired output voltage. Tied to an external pull−up resistor.
25	AV_{IN}	Input signal supply voltage pin.
26	FB1	Feedback Pin. Used to set the output voltage of Channel 1 with a resistive divider from the output.
27	AGND	Analog ground. Connect to GND1 and GND2.
28	COMP1	Compensation pin of Channel 1. This is the output of the error amplifier and inverting input of the PWM comparator.
29	SS1	Soft−start/stop control input for Channel 1. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
30	GND1	Power ground for Channel 1.
	Exposed Pad (GND)	The exposed pad at the bottom of the package is the electrical ground connection of the NCP3120. This node must be tied to ground.

Performance Information

The following Figures show typical performance of the NCP3120 in this evaluation board.

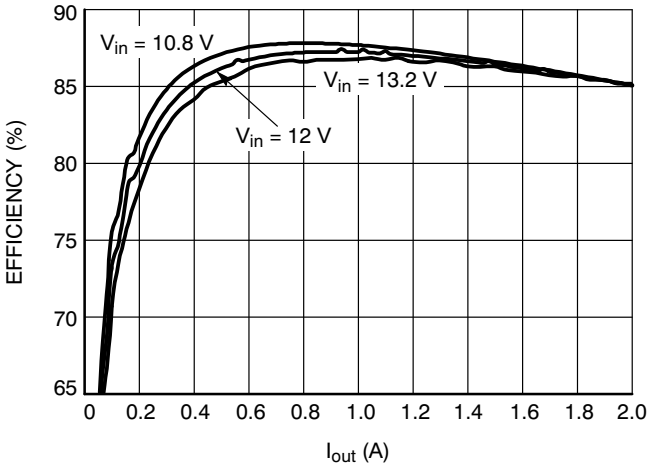

Figure 6. Efficiency for V_{out1} = 3.3 V

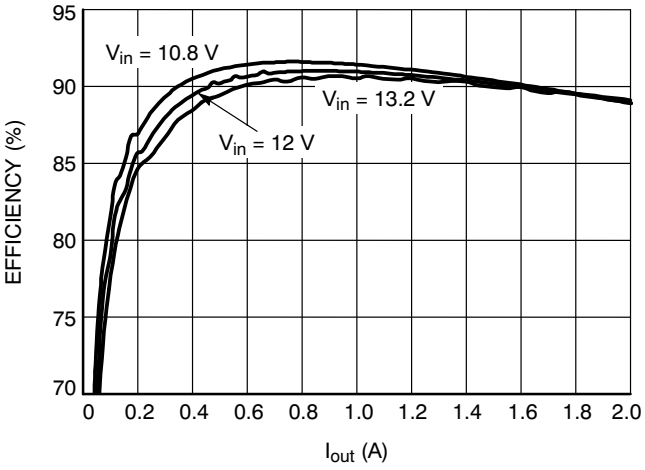

Figure 7. Efficiency @ V_{out2} = 5 V

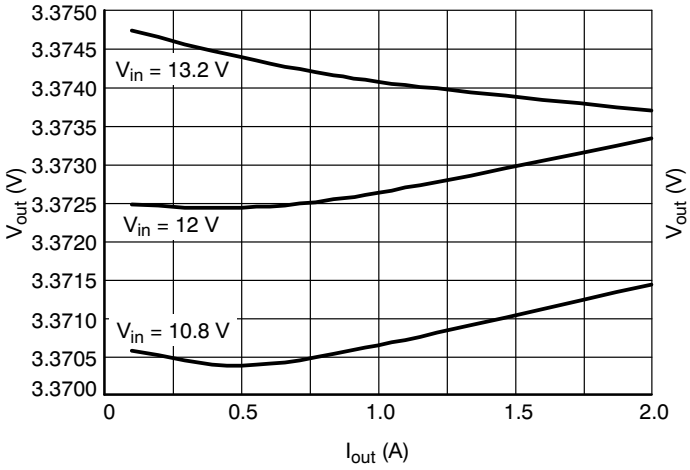

Figure 8. Load Regulation vs. V_{in} for V_{out1} = 3.3 V

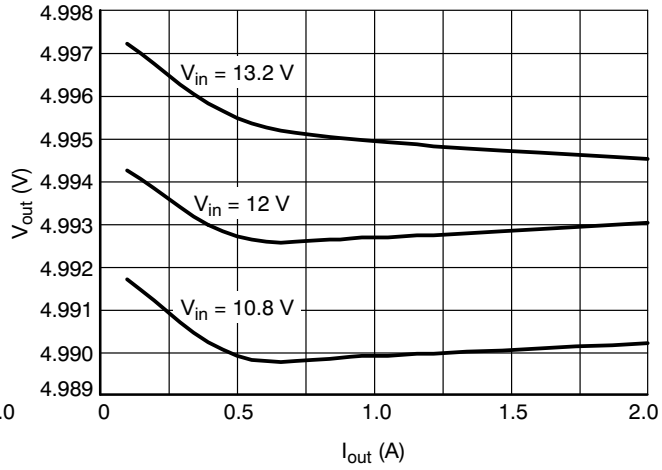

Figure 9. Load Regulation vs. V_{in} for V_{out1} = 3.3 V

Performance Information – cont.

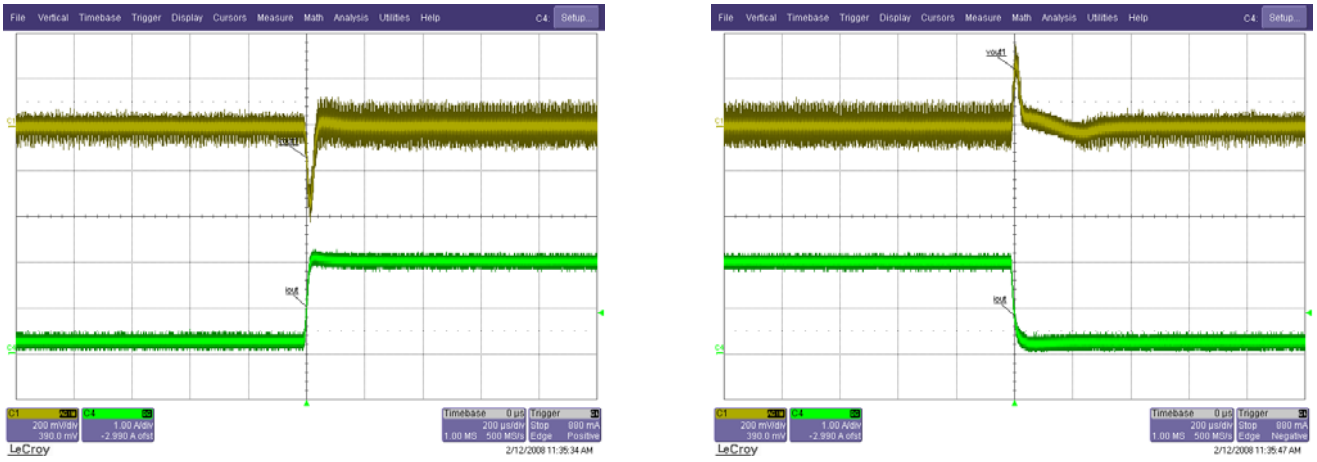

Figure 10. Load Transient – V_{out1} (V_{in} = 12 V, I_{out} = 200 mA –to– 2 A –to– 200 mA)
(CH1 = V_{out1}, CH4 = I_{out1})

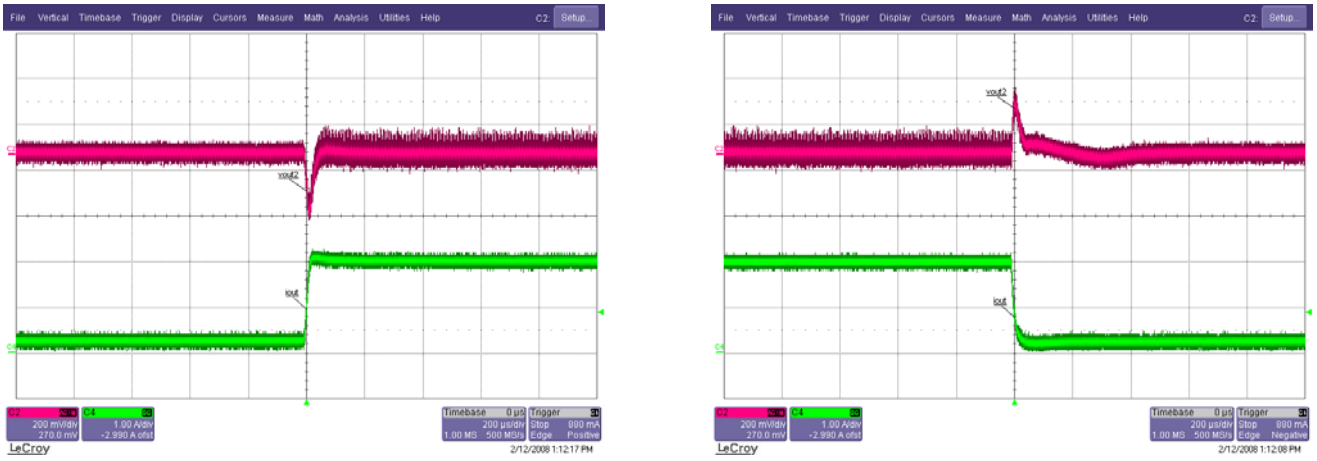

Figure 11. Load Transient – V_{out2} (V_{in} = 12 V, I_{out} = 200 mA –to– 2 A –to– 200 mA)
(CH1 = V_{out2}, CH4 = I_{out2})

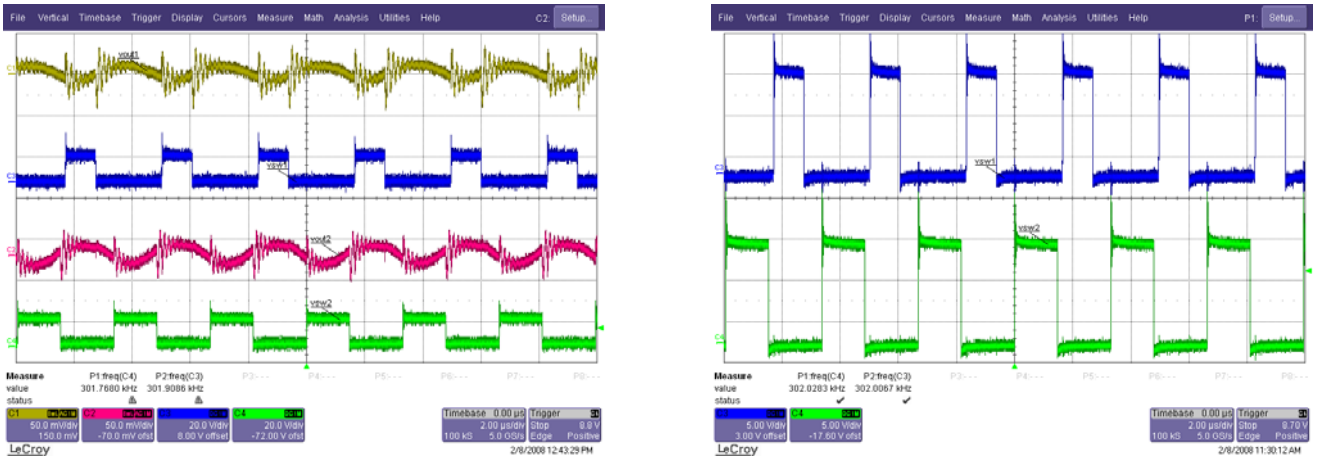

Figure 12. Switching Waveforms V_{out1}, V_{out2}, V_{SW1}, V_{SW2}
CH1 = V_{out1}, CH2 = V_{out2}, CH3 = V_{SW1}, CH4 = V_{SW2})

Performance Information − cont.

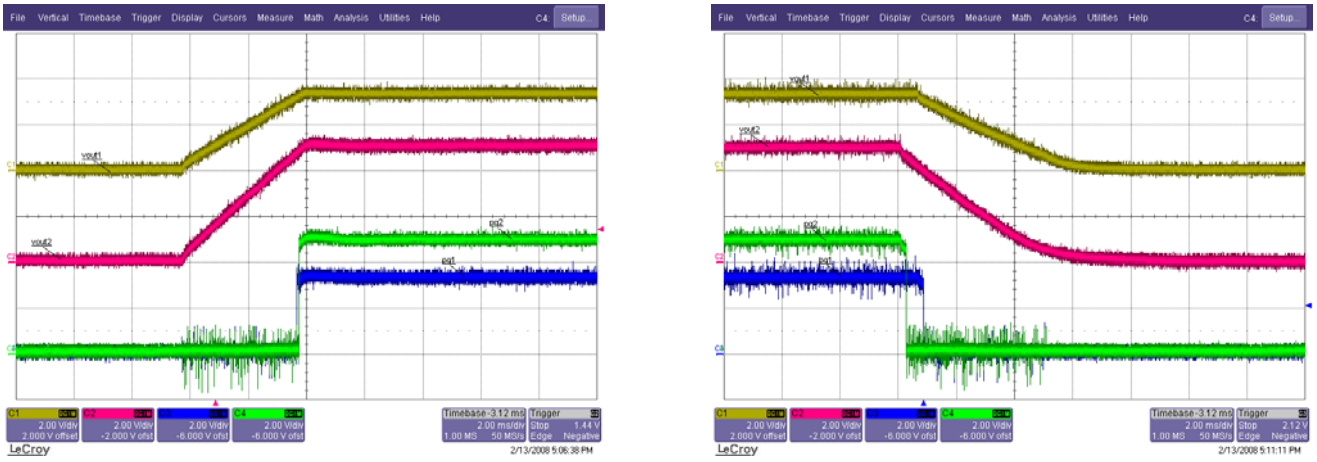

Figure 13. Ratiometric Startup of $V_{out1/2}$ with Power Good Outputs
(CH1 = V_{out1}, CH2 = V_{out2}, CH3 = PG1, CH4 = PG2)

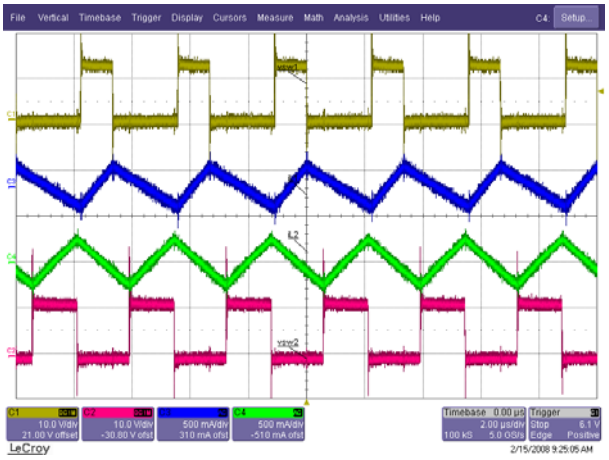

Figure 14. Switching Waveforms Showing 180° Phase Shift Operation
(CH1 = V_{SW1}, CH2 = V_{SW2}, CH3 = I_{L1}, CH4 = I_{L2})

Performance Information – cont.

Hiccup Overload Protection

The NCP3120 uses hiccup mode protection to protect the power supply from damage during overload conditions. During normal operation, the external soft start capacitor is pulled up by a current source that delivers 10 μA to the SS pin capacitor. This current source continues to charge the soft start capacitor until it reaches the saturation voltage of the current source (typically 4 V).

When the NCP3120 detects an overload condition (FB voltage falls to 0.5 V), switching stops, the soft start capacitor is discharged to 0.1 V and again charged to 1 V. The output of the error amplifier is also tied to ground (output transistor is closed) during the soft start capacitor discharge. If the output voltage is still below the overload condition voltage (0.5 V), the cycle repeats, as shown in Figure 15.

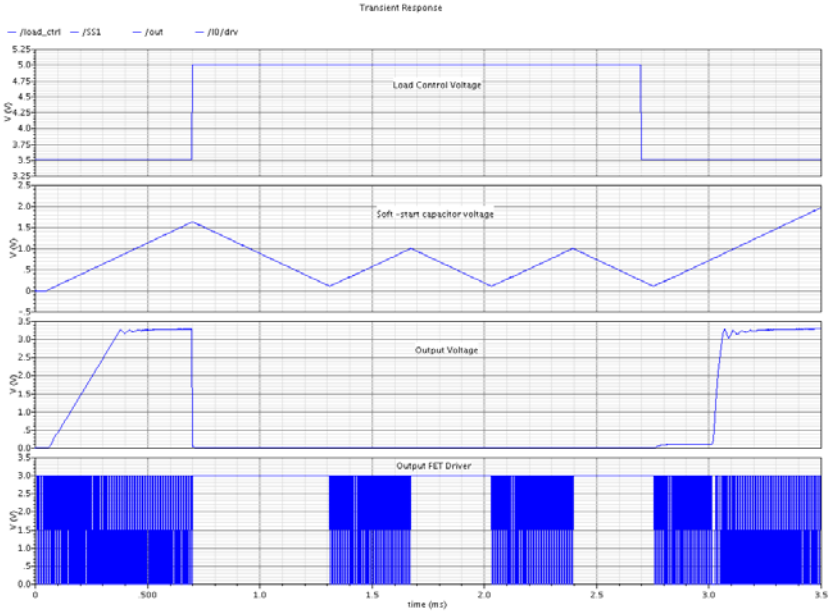

Figure 15. Hiccup Overload Protection Description (V_{in} = 12 V)

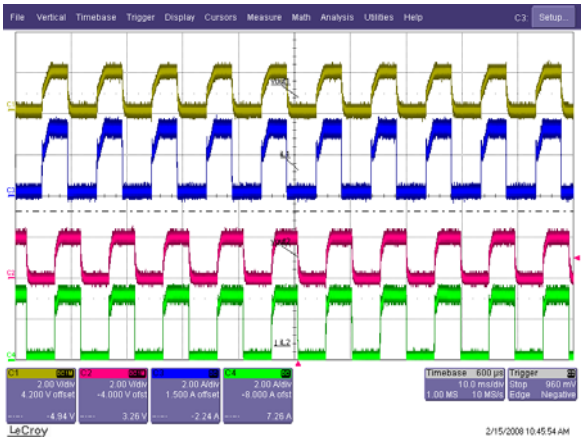

Figure 16. Switching Waveforms Showing Hiccup Overload Protection (CH1 = V_{SW1}, CH2 = V_{SW2}, CH3 = I_{L1}, CH4 = I_{L2})

Bill of Materials

Designator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer Part Number	Manufacturer
C1	1	Ceramic Chip Capacitor, 50 V	120 p	±10%	0603	VJ0603A121JXACW1BC	Vishay
C2	1	Ceramic Chip Capacitor, 50 V	22 n	±10%	0603	VJ0603Y223KXJCW1BC	Vishay
C3	1	Ceramic Chip Capacitor, 50 V	680 p	±10%	0603	C1608C0G2E681J	TDK
C4	1	Ceramic Chip Capacitor, 50 V	10 n	±10%	0603	VJ0603Y103KXACW1BC	Vishay
C5−6	2	Ceramic Chip Capacitor, 50 V	47 n	±10%	0603	C1608X7R1E473K	TDK
C7	1	Ceramic Chip Capacitor, 6.3 V	1 μ	±10%	0603	C1608X5R0J105K	TDK
C8	2	Ceramic Chip Capacitor, 50 V	1 n	±10%	0603	C1608C0G1H102J	TDK
C9, C20−21	3	Ceramic Chip Capacitor, 16 V	0.1 μ	±10%	0603	C1608X7R1C104K	TDK
C10	1	Ceramic Chip Capacitor, 50 V	120 p	±10%	0603	VJ0603A121JXACW1BC	Vishay
C11−C13	3	Aluminum Electrolytic	220 μF	±20%	HA0	EMZA250ADA221MHA0G	United Chemicon
C14−16, C19	4	Ceramic Chip Capacitor, 6.3 V	10 μF	±10%	0805	C2012X5R0J106M	TDK
C17−18	2	Ceramic Chip Capacitor, 16 V	10 μF	±10%	1206	C3216X5R0J106K	TDK
U1	1	Dual, 2A Buck Converter	−	−	QFN32, 5x5x1	NCP3120MNTXG	ON Semiconductor
D1−2	2	Schottky Power Rectifier	3 A 40 V	n/a	SMA	MBRA340T3	ON Semiconductor
R1	1	SMT Resistor	47.5 k	±1%	0603	CRCW060347K5FKEA	Vishay
R11	1	SMT Resistor	100	±1%	0603	CRCW0603100RFKEA	Vishay
R12	1	SMT Resistor	6.81 k	±1%	0603	CRCW06036K81FKEA	Vishay
R13−14	2	SMT Resistor	20	±5%	0603	CRCW060320R0JNEA	Vishay
R15	1	SMT Resistor	15	±1%	0603	CRCW060315R0FKEA	Vishay
R2	1	SMT Resistor	15 k	±1%	0603	CRCW060315K0FKEA	Vishay
R3	1	SMT Resistor	68.1 k	±1%	0603	CRCW060368K1FKEA	Vishay
R4	1	SMT Resistor	13 k	±1%	0603	CRCW060313K0FKEA	Vishay
R5	1	SMT Resistor	1 k	±1%	0603	CRCW06031K00FKEA	Vishay
R6	1	SMT Resistor	1.69 k	±1%	0603	CRCW06031K69FKEA	Vishay
R7	1	SMT Resistor	316 k	±1%	0603	CRCW0603316KFKEA	Vishay
R8−9	2	SMT Resistor	10 k	±1%	0603	CRCW060310K0FKEA	Vishay
R10	1	SMT Resistor	75 k	±1%	0603	CRCW060375K0FKEA	Vishay
L1−2	2	Inductor	22 μH	±20%	ER	IHLP4040DZER220M11	Vishay
EN FBB1−2 FBT1−2 VINT VOUT_1−2 VSW1−2	10	GENERIC 2 PIN SIP HEADER 0.100 CENTERS		n/a	0.100 Centers		
VIN VOUT1−2	3	4 PIN Connector	4	n/a	4 PIN Connector	1−640445−4	TYCO

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